First studies on the possibility to put control electronics inside the cryomodules

F. Scuri[a)]

for the ILC/Pisa working group

SMTF Workshop, Oct.5-7, 2005

Items:

- Motivations from a short list of the cryomodule internal components requiring read-out/control signals;
- A schematic description of a possible lay-out for a (full) internal electronics to handle all LV control signals of the cryomodule inner components.
- The results on power dissipation, timing performances, and costs after a quick search on the net for the required commercial electronic components.
- Some (encouraging) preliminary conclusions and a (may be incomplete) list of open problems
- Back-up material for component description.

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Motivation

- The large number of feed-troughs in the cryomodule is the main source of vacuum loss (less critical for cooling efficiency loss)
- No matter the final design will be, each cryomodule will contain several devices which must be powered, and controlled (or monitored)
- A sizable reduction factor (>> 2) in the number of feed-troughs would be useful and desired.

The basic initial idea: ➔design

- Low power dissipation
- Small volume
- Low cost
- Sufficiently fast (10-100 MHz)
- Multi-purpose

monitor/control electronics which can be integrated in a single card located just inside the external cryostat wall

➔Use a single serial data link for outside communication

Rationalization of the power line distribution is not (yet) considered here.

SOME REMARKS ON THE "EXTERNAL" "(ALMOST) FULL INTERNAL CONTROL" CONCEPT S

Assuming each module to contain (minimal assumption):

- ~ 10 cavities, ➔ ~10 pick-up signals
- fast and slow tuners, just 1 piezo and 1 stepping motor for each cavity, 2 control signals each tuner:
- ~ 10 LV control signals for sensors/actuators on BPM, QUAD & WPM (Wire Position Monitor) or any other system for alignment/vibration measurement
- ~ 10 LV monitor signals (Pressure, temp., vacuum,…)

➔ External control concept requires:

- ~10 ceramic (delicate) feed-troughs for RF cavity pick-ups
- "standard" feed-troughs for ~ 50 LV channels

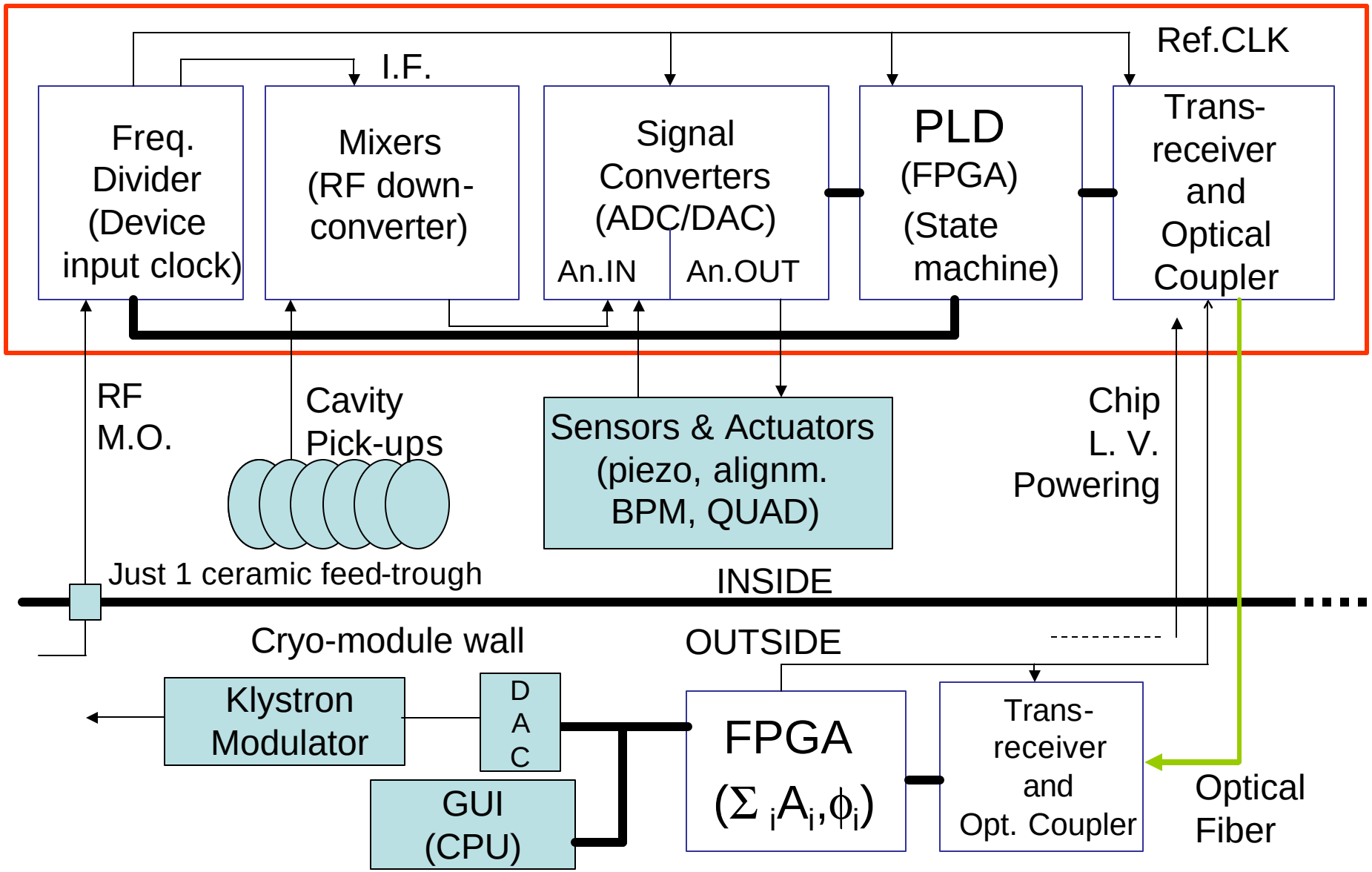
In principle, IF

- the frequency down-conversion and the A/D conversion of pick-ups and the control of all other cryomodule components can be made by a LPD inside the module,
- signals can be serial sent out via optical fiber or wireless

➔ Internal control concept would require:

- Just 1 ceramic (delicate) feed-trough (M.O. RF)
- A “standard” feed-trough for < 5 LV channels
- A single serial data link

Building-block diagram for control electronics inside a cryomodule



ADDITIONAL REMARKS ON THE "(ALMOST) FULL INTERNAL CONTROL" CONCEPT

1) The total power dissipation of the control electronics internal to the cryomodule must be minimized

2) A golden rule: power dissipation increases almost linear with frequency.

3) Latency introduced by additional (w.r.t external control concept) devices (serial interface,…) must be also minimized .

4) Evaluate 1) and 3) w.r.t. the fastest control/monitor signals:

- LLRF control (1 Msps, Simcom card @ Tesla)[a)]
- BPM monitor (10-100 Msps to achieve good bunch-to- bunch signal separation)[b)]

5) The Vector Sum could be implemented in the internal PLD used for all controls and avoid ~300 ns additional latency for LLRF control;

6) The remaining external FPGA/CPU/DAQ system can be eventually integrated in a commercial device.

a) S.Simrock, Snowmass 05

b) C. Adolphsen, Snowmass 05

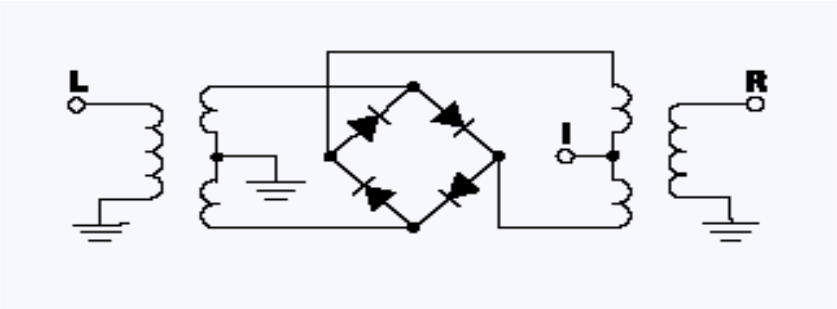
First evaluation of the main characteristics of the main components to be included in the internal control card. (after a quick survey of commercial devices on the net…)

1) Frequency dividers (1 unit in total):

Ref.Analog Device AD9510, Max. input freq. 1.6 GHz,
8 programmable outputs
Max. Power dissipation: 600 mW
Latency/delays: negligible (< 2 ns)
Unit price : < 15 USD

2) Mixers (1 per cavity):

Ref. Mini-Circuits, low level mixers, 2 to 12,000 MHz
Purely passive, ~50 mW max power dissipation



Unit price <=10 USD, total (~10 units) <= 100 USD

3) Signal converters :

Ref, Dallas Semiconductors, low power dissipation:
- Max1437 (fast for LLRF, 2 octal units , serial out
- Max1342 (slower, all other controls, <= 3 octal units

Type	bit	chs	Conv. Rate Min Msps	Max	Data Latency cycles	Max.Power dissipat. mW	Continuos power diss. mW@T=20C	derated mW/^{o}C
1437	12	8	4	50	6.5	882	~1500	47.6
1342	12	8[a)]	0.001	0.3	?	10	~ 700	26.3

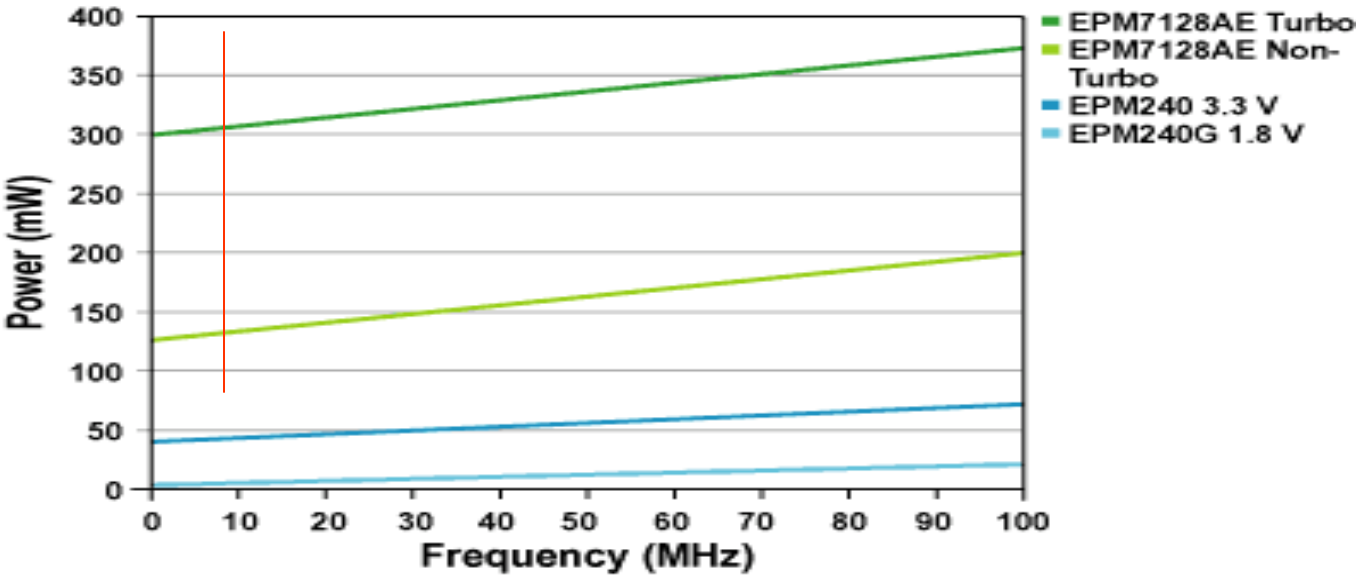
Operating temperature range: - 40 +85 ^{o}C

[a)] 4 additional DAQ chs.

Assuming to use :	Unit price (USD)
- 2 Max1437 units (LLRF, BPM)	49.85
- 3 Max1342 units (all other controls)	10.74
➔ Max total power dissipation ~ 7 Watt	
➔ Total cost for converters: ~ 150 USD	

4) Internal digital processor (LPD):

Ref. Altera MAX-II series (low power dissipation)



Max. power dissipation @ 10 MHz: ~ 300 mW

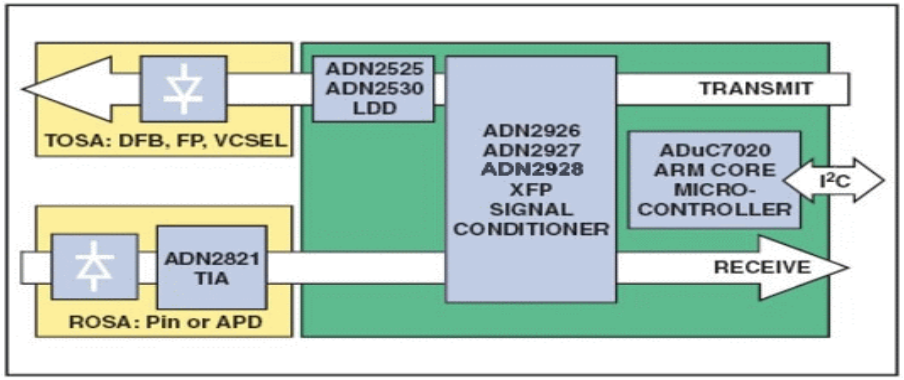
Latency : ~ 300-400 ns if Vector Sum is also performed (Tesla-Simcom experience), much less if only a few sequential FP operations are required

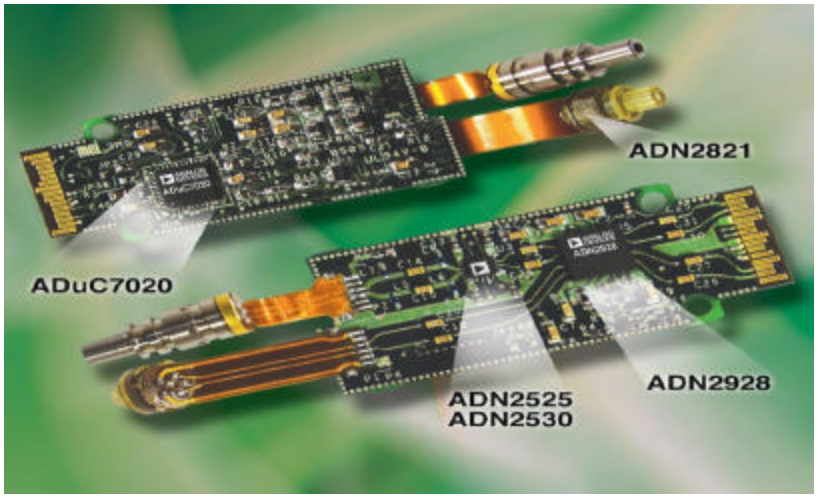
(internal clock up to 300 MHz ➔ < 200 ns latency for a 50 FP operation algorithm….)

Unit price:<= 50 USD

5) Internal Trans-receiver and optical coupler:

Ref. Analog Device XFP chipset (10GBps)





Device	Max.Pow.Diss. (mW)	Unit price (USD)
ADN2928	750	50
ADN2821	150	30
ADN2525	750	30
ADN2530	300	30
ADuC7020	150	15
Total	2100	155

Rough preliminary summary of the specs for the Internal Control Card

Device	Max. Power Diss. (total) Watt	Latency ns	Cost USD
Freq. Divider (1)	0.6	-----	15
Mixer (10)	0.5	-----	100
Signal Converters (2+3)	7.0	$(6.5/f_{samp})$[a)]	150
LPD (1)	0.3	300	50
TransReceiv./Opt.Coup.(1)	2.1	-----	150
Ancillary components[b)]	<10.0	-----	<500
Total	~ 20.0	<= 1µs	~1000

a) 600-700 ns @ 10 Msps, due to serial out; total latency could be reduced with a parallel-out converter and by making serialization in the PLD.

b) IC card, LV filters (capacitors), line drivers, sync. logic (shift registers, buffers ext. to the LPD….)

Preliminary conclusions:

- The Internal Control Card is low cost, small volume (all components can be hosted on a ~ 10x10 cm^2 IC card)
- Total power dissipated by the operating card is negligible compared to the total Black Body radiation inside the cryomodule.; the irradiation fraction of the power locally dissipated (total average density ~2000 W/m^2) is similar to the Black Body radiation density on the inner surface of the cryomod. wall (~500 W/m^2 @ T = 20 ^oC)
- Maximum total latency (1 μs) is still compatible with the timing requirements of the TESLA LLRF control model
- All components for the internal control card can operate down to -40 ^oC.

➔ The idea seems not too naïve, further studies are required……

Moreover:

- The internal control should allow more flexibility in extending the number of controls that can be done
- No relevant changes in the design and in the HW (costs) should be required to follow upgrades in machine energy

To do and open problems:

- Experts will review component compatibility for a more refined design of the card;

- Radiation hardness of the devices must be studied; all components are implemented with CMOS technology….

- When module design and cable plant in the module will be more defined the correct evaluation of the channel number for LV controls could let vary the estimations quoted here, much less than 1 order of magnitude anyway….

-The presented "concept" of the internal control logic must be carefully reviewed for a better evaluation of pro and contra;

- Eventually LLRF could be separated from the other controls, acting the control loop on components external to the cryomodule too (Klystron modulator).

- A design for the mechanics to hold (on a plug-in flange ?) is required.

Acknowledgments

This work has been done with the assistance of **S.Galeotti** and **F.Spinella** of the Electronic Engineering Department of INFN-Pisa.
Their support is expected for future detailed engineering of this project.

Useful suggestions came from the other working-group members:

F.Bedeschi (INFN-Pisa)
G.Bellettini (Scuola Normale Superiore – Pisa)
R.Carosi (INFN-Pisa)
M.Carpinelli (INFN-Pisa)
C.Paglairone (Univ. Cassino)

BACK_UP

AD9510 - 1.2 GHz Clock Distribution IC, PLL Core, Dividers, Delay Adjust, Eight Outputs

The AD9510 provides a multi-output clock distribution function along with an on-chip PLL core. The design emphasizes low jitter and low phase noise in order to maximize data converter clocking.

Two evaluation boards are available for the AD9510:
AD9510/PCB: Evaluation Board without VCO or VCXO or loop filter
AD9510-VCO/PCB: Evaluation Board with 245.76MHz VCXO, loop filter

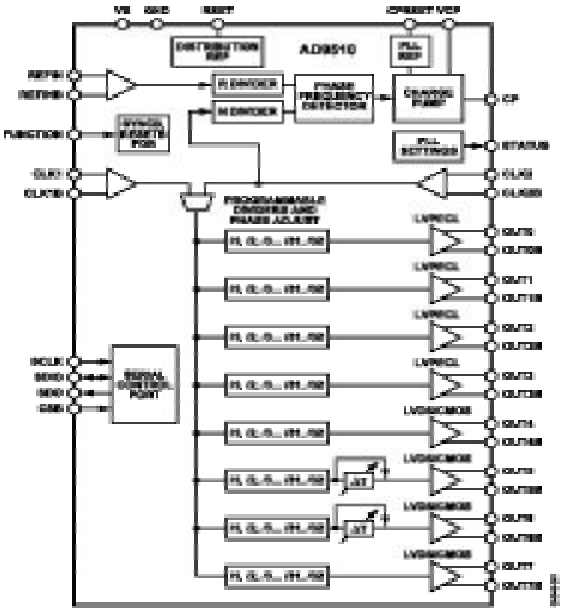
An Overview of the Clock Distribution/Generation Family is available.

Specifications

Clk_func	Distribution
OnChip_Multiplier	PLL Core
+Supply_V	3.3V
F-in_max	1.6GHz
Outputs	8
f-out_max	1.2GHz
Random_jitter_ps-rms	0.25 Additive
I/O_Interface	Serial
Pkg	64-LFCSP
Output_Logic	CMOS, LVDS, LVPECL
prod_descrip	1.2 GHz,Ultra-Low Jitter Clock Distribution IC w/ Dividers, PLL Core, Delay Adj. & 8 Outputs

Find Similar Products

Functional Block Diagram



Phase locked loop (PLL) Core
Reference input frequencies to 250 MHz Programmable dual-modulus prescaler Programmable charge pump (CP) current Separate CP supply (VCP) extends tuning range
Two 1.6 GHz, differential clock inputs
8 programmable dividers, 1 to 32, all integers
Phase select for output-to-output coarse delay adjust

Four independent 1.2 GHz LVPECL outputs
Additive output jitter , 225 fs RMS
Four independent 800 MHz/250 MHz LVDS/CMOS outputs
Additive output jitter, 275 fs RMS Fine delay adjust on 2 outputs, 5-bit delay words
Serial control port
Space-saving 64-lead LFCSP

FREQUENCY MIXERS *Surface Mount*

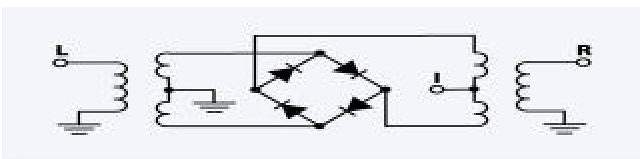
LOW LEVEL 2 to 12000 MHz

MODEL NO.	LO LEVEL (dBm)	RF @ 1dB Comp. Typ. (dBm)	FREQUENCY MHz LO/RF f_L-f_U	FREQUENCY MHz IF	CONVERSION LOSS dB $\bar{x}$	σ	Max.	Total Range Max.	LO-RF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	IP3@ center band Typ. (dBm)	E factor	CASE STYLE	CONNECTION	PCB Lay-out PL-	PRICE $ ea. Qty. (10-49)
◆ ADE-1L**	+3	0	2-500	DC-500	5.2	0.1	7.2	8.0	68	50	55	30	44	30	55	40	45	30	35	25	16	1.3	CD542	nt	052	3.95
◆ ADEX-10L**	+4	+1	10-1000	DC-800	7.2	0.1	8.2	8.8††	75	55	60	40	47	37	40	26	33	20	24	13	16	1.2	CD542	nt	052	2.95
◆ MBA-10L*	+3	0	800-1000	DC-200	8.0	0.1	—	9.5	20 (typ.) 13 (min.)						15 (typ.) 8 (min.)						9	0.6	SM2	ld	066	6.95
◆ MBA-15L*	+4	0	1200-2400	DC-600	6.5	0.1	—	8.5	27 (typ.) 14 (min.)						14 (typ.) 8 (min.)						10	0.6	SM2	ld	066	6.95
◆ MBA-25L*	+4	0	2000-3000	DC-600	6.2	0.15	—	8.6	28 (typ.) 18 (min.)						15 (typ.) 7 (min.)						10	0.6	SM2	ld	066	6.95
◆ MBA-591L*	+4	+1	4950-5900	DC-1000	7.0	0.1	—	9.0	35 (typ.) 25 (min.)						26 (typ.) 17 (min.)						15	1.1	SM2	le	067	6.95
NEW◆ MCA1-85L	+4	0	**2800-8500**	**DC-1200**																						
			2800-5000	DC-1200	5.7	0.2	8.4¹	—	35 (typ.) 20 (min.)						13 (typ.) 7 (min.)						11	0.7	DZ885	ld	045	9.45
			5000-7500	DC-1200	6.0	0.3	8.4¹	—	35 (typ.) 20 (min.)						38 (typ.) 20 (min.)						7	0.3				
			7500-8500	DC-1200	7.0	0.3	—	—	31 (typ.) —						32 (typ.) —						8	0.4				
NEW◆ MCA1-12GL	+4	+1	**3800-12000**	**DC-1500**																						
			3800-6500	DC-1500	6.8	0.2	8.5¹	—	32 (typ.) 17 (min.)						13 (typ.) 8 (min.)						9	0.5	DZ885	ld	045	11.95
			6500-9500	DC-1500	6.5	0.3	9.2¹	—	38 (typ.) 24 (min.)						40 (typ.) 20 (min.)						7	0.3				
			9500-12000	DC-1500	7.0	0.3	—	—	25 (typ.) 17 (min.)						26 (typ.) 15 (min.)						6	0.2				Qty. (1-9)
RMS-5L	+3	-3	400-1400	DC-800	7.0	0.2	—	9.8	22 (typ.) 14 (min.)						22 (typ.) 6 (min.)						9	0.2	TT240	w	052	13.95

E= [IP3(dBm)-LO Power(dBm)]/10

L = low range [f_L to 10 f_L] M = mid range [10 f_L to f_U/2] U = upper range [f_U/2 to f_U]

m = mid band [2f_L to f_U/2]



NOTES:

- $\bar{x}$ Average of conversion loss at center of mid-band frequency (f_L+f_U/4)
- σ Standard deviation
- ◆ Aqueous washable.
- † Phase detection, positive polarity.
- * BLUE CELL™ mixers protected by U.S. Patents 5,534,830 5,640,132 5,640,134 5,640,699
- ** Protected under U.S. patent 6133525
- †† Conversion loss increases 0.8 dB when IF is above 150 MHz.
- ¹ Conversion loss at 30 MHz IF, increases with IF frequency.
- A. Environmental specifications and re-flow soldering information available in General Information Section.
- B. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Drawings".
- C. Prices and Specifications subject to change without notice.
- 1. Absolute maximum power, voltage and current ratings:
  - 1a. RF power, 50mW
  - 1b. Peak IF current, 40mA

pin connections

PORT	w	nt¹	ld	le
LO	1	6	10	10
RF	4	3	5	6
IF	5	2	3	1
GND EXT.	2,3,6	1,4,5	all others	all others
DEMO BOARD	TB-03	TB-03	TB-99(MBA) TB-144(MCA1)	TB-74

¹ pin connection physically same as w

041210

19-3645; Rev 0; 4/05

EVALUATION KIT AVAILABLE

Octal, 12-Bit, 50Msps, 1.8V ADC with Serial LVDS Outputs

MAX1437

General Description

The MAX1437 octal, 12-bit analog-to-digital converter (ADC) features fully differential inputs, a pipelined architecture, and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power and high-dynamic performance in medical imaging instrumentation and digital communications applications. The MAX1437 operates from a 1.8V single supply and consumes only 768mW (96mW per channel) while delivering a 69.9dB (typ) signal-to-noise ratio (SNR) at a 5.3MHz input frequency. In addition to low operating power, the MAX1437 features a power-down mode for idle periods.

An internal 1.24V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure allows the use of an external reference for applications requiring increased accuracy or a different input voltage range. The reference architecture is optimized for low noise.

A single-ended clock controls the data-conversion process. An internal duty-cycle equalizer compensates for wide variations in clock duty cycle. An on-chip PLL generates the high-speed serial low-voltage differential signal (LVDS) clock.

The MAX1437 has self-aligned serial LVDS outputs for data, clock, and frame-alignment signals. The output data is presented in two's complement or binary format.

The MAX1437 offers a maximum sample rate of 50Msps. See the *Pin-Compatible Versions* table below for higher- and lower-speed versions. This device is available in a small, 14mm x 14mm x 1mm, 100-pin TQFP package with exposed paddle and is specified for the extended industrial (-40°C to +85°C) temperature range.

Applications

Ultrasound and Medical Imaging

Instrumentation

Multichannel Communications

Features

- **Excellent Dynamic Performance**
  69.9dB SNR at 5.3MHz
  96dBc SFDR at 5.3MHz
  95dB Channel Isolation
- **Ultra-Low Power**
  96mW per Channel (Normal Operation)
- **Serial LVDS Outputs**
- **Pin-Selectable LVDS/SLVS (Scalable Low-Voltage Signal) Mode**
- **LVDS Outputs Support Up to 30 Inches FR-4 Backplane Connections**
- **Test Mode for Digital Signal Integrity**
- **Fully Differential Analog Inputs**
- **Wide Differential Input Voltage Range (1.4VP-P)**
- **On-Chip 1.24V Precision Bandgap Reference**
- **Clock Duty-Cycle Equalizer**
- **Compact, 100-Pin TQFP Package with Exposed Paddle**
- **Evaluation Kit Available (Order MAX1437EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1437ECQ	-40°C to +85°C	100 TQFP-EP* (14mm x 14mm x 1mm)

**EP = Exposed paddle.*

Pin-Compatible Versions

PART	SAMPLING RATE (Msps)	RESOLUTION (BITS)
MAX1434	50	10
MAX1436	40	12
MAX1438**	65	12

***Future product—contact factory for availability.*

Pin Configuration appears at the end of data sheet.

19-3332; Rev 1; 8/04

EVALUATION KIT AVAILABLE

MAXIM

12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

General Description

The MAX1340–MAX1343/MAX1346–MAX1349 integrate a multichannel, 12-bit, analog-to-digital converter (ADC) and a quad, 12-bit, digital-to-analog converter (DAC) in a single IC. The devices also include a temperature sensor and configurable general purpose I/O ports (GPIOs) with a 25MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. The ADC is available in a 4 or an 8 input-channel version. The four DAC outputs settle within 2.0µs, and the ADC has a 300ksps conversion rate.

All devices include an internal reference (2.5V or 4.096V) providing a well-regulated, low-noise reference for both the ADC and DAC. Programmable reference modes for the ADC and DAC allow the use of an internal reference, an external reference, or a combination of both. Features such as an internal ±1°C accurate temperature sensor, FIFO, scan modes, programmable internal or external clock modes, data averaging, and AutoShutdown™ allow users to minimize both power consumption and processor requirements. The low glitch energy (4nV•s) and low digital feedthrough (0.5nV•s) of the integrated quad DACs make these devices ideal for digital control of fast-response closed-loop systems.

The devices are guaranteed to operate with a supply voltage from +2.7V to +3.6V (MAX1341/MAX1343/MAX1347/MAX1349) and from +4.5V to +5.5V (MAX1340/MAX1342/MAX1346/MAX1348). The devices consume 2.5mA at 300ksps throughput, only 22µA at 1ksps throughput, and under 0.2µA in the shutdown mode. The MAX1342/MAX1343/MAX1348/MAX1349 offer four GPIOs that can be configured as inputs or outputs.

The MAX1340–MAX1343/MAX1346–MAX1349 are available in 36-pin thin QFN packages. All devices are specified over the -40°C to +85°C temperature range.

Applications

Closed-Loop Controls for Optical Components and Base Stations

System Supervision and Control

Data-Acquisition Systems

Features

- 12-Bit, 300ksps ADC
  - Analog Multiplexer with True-Differential Track/Hold (T/H)
  - 8 Single-Ended Channels or 4 Differential Channels (Unipolar or Bipolar)
  - 4 Single-Ended Channels or 2 Differential Channels (Unipolar or Bipolar)
  - Excellent Accuracy: ±0.5 LSB INL, ±0.5 LSB DNL
- 12-Bit, Quad, 2µs Settling DAC
  - Ultra-Low Glitch Energy (4nV•s)
  - Power-Up Options from Zero Scale or Full Scale
  - Excellent Accuracy: ±0.5 LSB INL
- Internal Reference or External Single-Ended/Differential Reference
  - Internal Reference Voltage 2.5V or 4.096V
- Internal ±1°C Accurate Temperature Sensor
- On-Chip FIFO Capable of Storing 16 ADC Conversion Results and One Temperature Result
- On-Chip Channel-Scan Mode and Internal Data-Averaging Features
- Analog Single-Supply Operation
  - +2.7V to +3.6V or +4.75V to +5.25V
- 25MHz, SPI/QSPI/MICROWIRE Serial Interface
- AutoShutdown Between Conversions
- Low-Power ADC
  - 2.5mA at 300ksps
  - 22µA at 1ksps
  - 0.2µA at Shutdown
- Low-Power DAC: 1.5µA
- Evaluation Kit Available (Order MAX1258EVKIT)

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Pin Configurations appear at end of data sheet.

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	REF VOLTAGE (V)	ANALOG SUPPLY VOLTAGE (V)	RESOLUTION BITS***	ADC CHANNELS	DAC CHANNELS	GPIOs
MAX1340BETX	-40°C to +85°C	36 Thin QFN-EP**	4.096	4.75 to 5.25	12	8	4	0
MAX1341BETX*	-40°C to +85°C	36 Thin QFN-EP**	2.5	2.7 to 3.6	12	8	4	0
MAX1342BETX	-40°C to +85°C	36 Thin QFN-EP**	4.096	4.75 to 5.25	12	8	4	4
MAX1343BETX*	-40°C to +85°C	36 Thin QFN-EP**	2.5	2.7 to 3.6	12	8	4	4

*Future product—contact factory for availability.
**EP = Exposed pad.
***Number of resolution bits refers to both DAC and ADC.

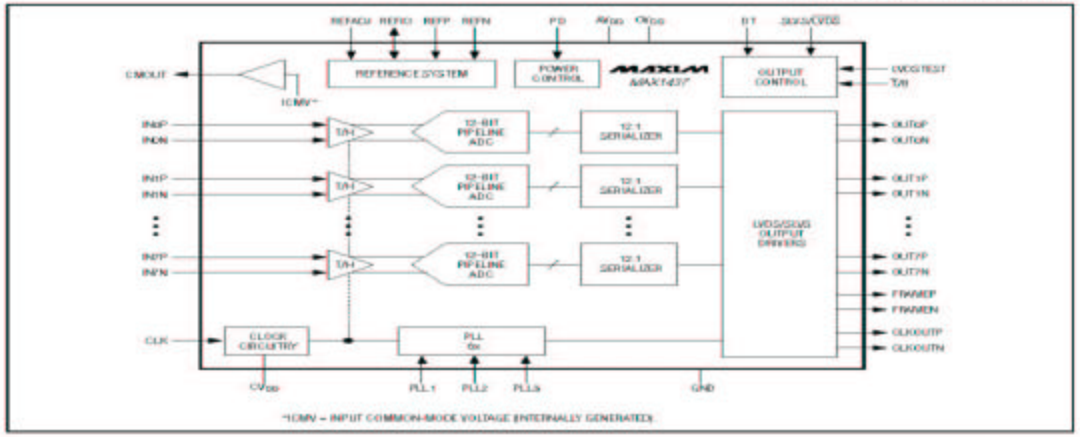
Ordering Information/Selector Guide continued at end of data sheet.

Signal converters layouts:

Octal, 12-Bit, 50Msps, 1.8V ADC with Serial LVDS Outputs

MAX1437

Functional Diagram



12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

MAX1340–MAX1343/MAX1346–MAX1349

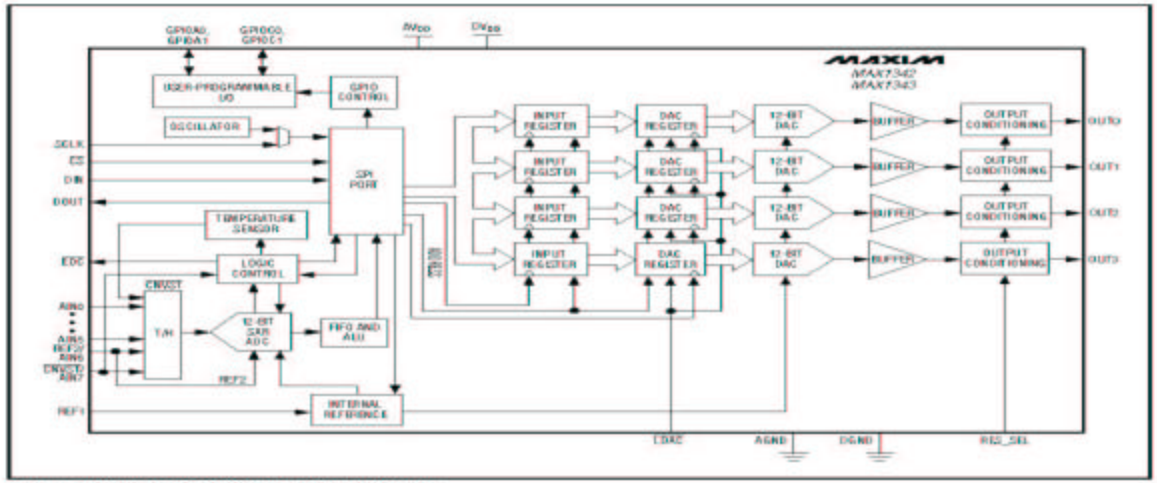
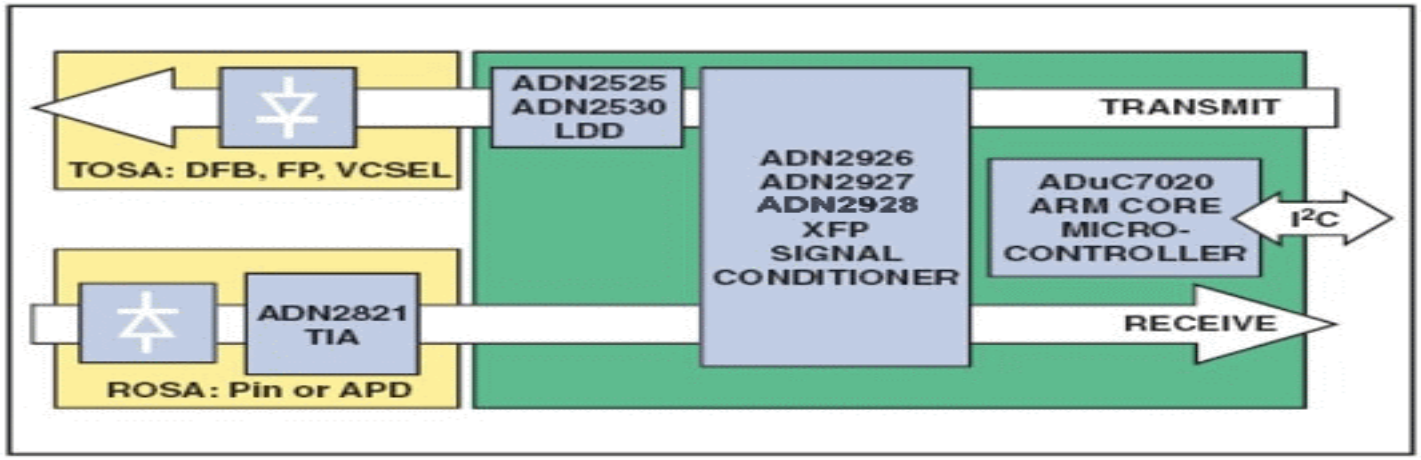


Figure 1. MAX1342/MAX1343 Functional Diagram

XFP Chipset and Reference Design Simplify 10 Gbps Transceivers



Analog Devices introduces a 10 Gbps chipset that offers low power and the highest performance for receive sensitivity and transmit eye quality. Best in class jitter performance of the XFP signal conditioner increases robustness and minimizes interoperability issues. The companion reference design simplifies evaluation and speeds time to market. The reference design includes XFP boards, Gerber files, microcontroller software, and a GUI interface.

Features

- 9.9 Gbps to 11.1 Gbps data rate
- DFB, FP, or VCSEL operation
- Exceeds 20% SONET optical eye margin over temperature
- -19 dBm receive sensitivity
- Unparalleled jitter performance
- Supports full digital diagnostics

- ADN2821 *ADPs and pins in standard low cost TO-46 cans*
  - -19 dBm sensitivity
  - 700 nA integrated input noise
  - 8.5 Gbps BW
  - 3.3 V, 150 mW
  - Supports APD or PIN diodes
  - RSSI power meter
  - 0.7 mm x 1.2 mm die size
  - Samples in die or ROSA format

ADN2928 Family of XFP Signal Conditioners
- 9.9 Gbps to 11.1 Gbps
- Exceeds XFP requirements for jitter at OC-192
- Lowest jitter generation: 6 mUI rms jitter
- Highest jitter tolerance: 0.6 UI p-p @ 10 MHz
- Lowest jitter transfer: 2.0 MHz OC-192
- ADN2928 transceiver in 6 mm x 6 mm BGA
- ADN2927 / ADN2926 standalone transmit and receive functions in a 4 mm x 4 mm LFCSP

ADN2525 Differential Active Backmatch LDD
- 9.9 Gbps to 10.7 Gbps
- DFB, FP, or VCSEL operation
- Superior optical eye margins
- SONET >20% over temperature
- Ethernet >40% over temperature
- 750 mW typ (laser + LDD) over temperature
- Active load improves impedance matching
- 3.3 V operation, 3 mm x 3 mm LFCSP

ADN2530 Differential Active Backmatch VCSEL Driver
- 9.9 Gbps to 10.7 Gbps
- 300 mW typ (laser + LDD) over temperature
- SONET eye margin exceeds 20%
- Crosspoint adjust feature
- Active load improves impedance matching
- 3.3 V operation, 3 mm x 3 mm LFCSP